of the first conductive typ , and a gat electrode that is disposed between said source and drain diffusion layers; and

a dopant diffusion region of a second conductive type that is set at a distance from said plurality of field effect transistors,

wherein said dopant diffusion region is connected to a reference potential,

wherein the drain diffusion layer is connected directly to an input/output terminal section without an intervening resistance element, and

wherein a first conductive type well having a lower dopant concentration than the source diffusion layer is formed under the source diffusion layer.

2. (Twice Amended) The semiconductor device according to Claim 1, wherein said gate electrode and said dopant diffusion region of the second conductive type are disposed over a second conductive type well that is formed on the surface of the semiconductor substrate, and

wherein the bottom of said first conductive type well is formed at the same depth as the bottom of the second conductive type well or at a level deeper than the bottom of the second conductive type well.

3. (Amended) The semiconductor device according to Claim 1, wherein said plurality of field effect transistors are N-channel type field effect transistors.

4. (Twice Amended) A semiconductor device having, on a semiconductor substrate, an input/output protection circuit section, the input/output protection circuit section comprising a complementary field effect transistor including a first field effect transistor having a source diffusion layer of a first conductive type, a drain diffusion layer of the first conductive type, and a gate electrode that is disposed between the source and drain diffusion layers of the first conductive type, and a second field effect transistor having a source diffusion layer of a second conductive type, a drain diffusion layer of the second conductive type, and a gate electrode that is disposed between the sourc and drain diffusion layers of the second conductive type,

wherein a first dopant diffusion region of the second conductive type is set at a distance from said first field effect transistor, and a second dopant diffusion region of the first conductive type is set at a distance from said second field effect transistor,

wherein the first dopant diffusion region is connected to a first reference potential, the second dopant diffusion region is connected to a second reference potential,

wherein the drain diffusion layer of the first field effect transistor and the drain diffusion layer of the second field effect transistor are each connected directly to an input/output terminal section without an intervening resistance element, and

wherein under the source diffusion layer of the first field effect transistor there is formed a first conductive type well having a lower dopant concentration than the source diffusion layer of the first field effect transistor.

5. (Twice Amended) The semiconductor device according to Claim 4, wherein the gate electrode of the first field effect transistor and the first dopant diffusion region are disposed over a second conductive type well that is formed on the surface of the semiconductor substrate, and

wherein the bottom of said first conductive type well is formed at the same depth as the bottom of the second conductive type well or at a level deeper than the bottom of the second conductive type well.

6. (Twice Amended) The semiconductor device according to Claim 5, wherein, beneath the second conductive type well, there is set a dopant high-concentration region containing second conductive type dopants with a higher dopant concentration than the second conductive type well, and

wherein the bottom of said first conductive type well is formed at the same depth as the bottom of said dopant high-concentration region or at a level deeper than the bottom of said dopant high-concentration region.

7. (Amended) The semiconductor device according to Claim 4, wherein the first field effect transistor is an N-channel type field effect transistor.

8. (Amended) A semiconductor device having an input/output protection circuit section on a semiconductor substrate, the input/output protection circuit section comprising:

a plurality of field effect transistors connected in parallel, each of which has a source diffusion layer of a first conductive type and a drain diffusion layer of the first conductive type and a gate electrode that is disposed between said first and second diffusion layers; and

a dopant diffusion region of a second conductive type that is set at a distance from said plurality of field effect transistors,

wherein said dopant diffusion region is connected to a reference potential,

wherein the drain diffusion layer is connected directly to an input/output terminal section without an intervening resistance element,

wherein a first conductive type well with a lower dopant concentration than the source diffusion layer is formed under the source diffusion layer, and

wherein the first conductive type well at least partially underlies an element isolation film separating the source diffusion area from the dopant diffusion region of the second conductive type.

REMARKS

The 5 November 2002 official action addressed claims 1-8. Claims 1-2, 4-6 and 8 are amended. Claims 1-8 are pending.

Claim amendments

The claims are amended to improve their language. The independent claims are further amended to specify that a drain diffusion of a field effect transistor is directly connected to an input section terminal without an intervening resistance element, as illustrated in the embodiments of the present application such as that of Figur 2.